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# No. 4 ESS:

# Mass Announcement Subsystem

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*This paper describes a new hardware subsystem developed to provide mass announcement capabilities for No. 4* ESS. *The subsystem records, stores, and plays back recorded announcements for distribution through the No. 4* ESS *switching network. Announcements are stored in digital form on a moving-head disk system. Microprocessors are used for control of disks and of interfaces. Duplicated hardware ensures high reliability, and extensive self-testing capability is provided.*

## I. INTRODUCTION

Provision of the mass announcement capability on the No. 4 Electronic Switching System (ESS) requires the system to record and store voice announcements, and to play them back to large numbers of calling customers. The capability of instantaneously creating multiple copies of an announcement and distributing the copies to many callers is inherent in the design of the No. 4 ESS digital switching network,[1] and is a principal reason for choosing No. 4 ESS as the vehicle for the mass announcement service. Recorded announcement hardware already in No. 4 ESS lacked the capacity and features needed, so a new hardware subsystem was designed.

This paper describes the hardware subsystem portion of the No. 4 ESS mass announcement capability. An overview of the entire capability, including No. 4 ESS processor software and interactions with the telephone network, appears in a companion paper.[2]

Architecture of the new mass announcement subsystem is influenced by the existing No. 4 ESS architecture and interfaces, and the functional

requirements and reliability objectives of the new service. For example, control information between the No. 4 ESS processor and the mass announcement subsystem is carried via the Peripheral Unit Bus (PUB) system whicb is used as the interface to the switching network and transmission interface equipment. This bus interface requires equipment similar to that used in other No. 4 ESS peripheral hardware frames, such as the Digital Interface (DIF) frame.[3] The simplest interface for voice signals to the all-digital No. 4 ESS switching network is the serial digital pulse code modulation (PCM) encoded format used for internal transmission within the No. 4 ESS network. This format was chosen for the recording and playback interface, and for storing the recorded announcements.

Figure 1 shows the major components of the mass announcement subsystem. Access to the No. 4 ESS processor is via the Peripheral Unit Control (PUC) equipment frame, which provides a standard bus interface plus control circuitry and programs to allow one PUC to serve one or two Mass Announcement System (MAS) frames and, potentially, also to serve additional frames containing features yet to be designed.

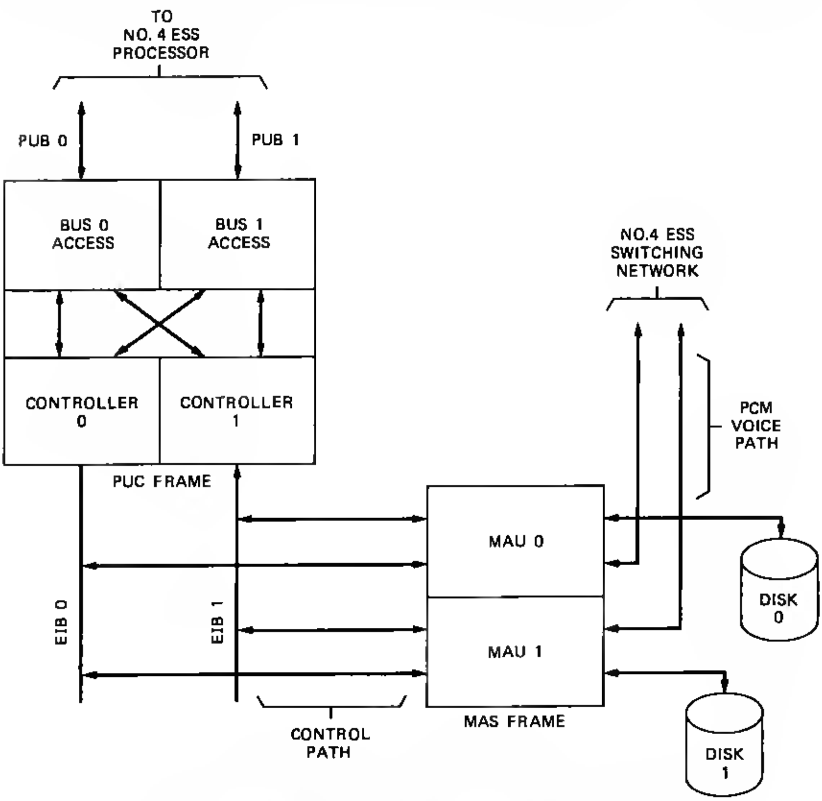


Fig. 1—Mass announcement subsystem bock diagram.

The PUC's full duplex bus interface and duplex controllers allow full service to continue even if an internal PUC unit fails.

Recording and distribution of announcements is performed by the MAS frame (Fig. 1). This frame contains two identical Mass Announcement Units (MAUs). Each has a disk controller and is associated with an 80-Mbyte moving-head disk system for announcement storage. In contrast to the PUC, whose duplex controllers perform identical tasks in synchronism, the two MAS disk controllers operate independently. All announcements are stored on both disks, however, so that if one unit is lost, all announcements remain available. A temporary service requiring longer customer waiting time for an announcement to start is provided in such cases.

In both the PUC and MAS frames, microprocessor systems are used extensively. Both the MAS disk controller, which controls data flow to and from the disks, and the PUC executive controller, which governs PUC internal data movements and the interface to MAS, are high-speed bipolar bit-sliced microprocessors. The PUC also contains a slower *BELLMAC*®-8 microprocessor for background maintenance tasks, and initialization.

## II. SYSTEM INTERFACES

A number of external and internal interfaces exist in the mass announcement subsystem (Fig. 1). This results from the structure of No. 4 ESS and from the characteristics of the PUC and MAS frames.

Voice signals for recording and playback of announcements are sent via a coaxial DS-120 high-speed serial PCM data link between each MAS unit and the switching and permuting circuit (SPC), that serves the MAS unit in a Time-Slot Interchange (TSI) frame in the No. 4 ESS network. Each link provides 120 two-way voice and eight maintenance channels. Sixty channels are used for playback, including certain channels reserved as "monitor channels" for verifying announcement integrity after recording. Fourteen channels are used for recording, and certain other channels are used for maintenance purposes. The interface carries no control information other than for timing and synchronizing the link itself.

Control information for the subsystem is carried via the PUB from the No. 4 ESS processor to the PUC frame. This is a 96-bit (total both directions) parallel interface under control of tbe processor. Frames are addressed via coded enabling bit fields on the bus. A wide variety of operational and maintenance orders destined for the PUC frame and, via the PUC, for the MAS frame are sent over this interface.

Additional external interfaces to the subsystem include dc loop and ac pulse leads from No. 4 ESS signal processor frames. These links are

used to monitor the status of both PUC and MAS frames, and to provide certain subsystem configuration functions. Finally, the PUC receives timing information from TSI frames.

Within the subsystem, the major interface involves the PUC and MAS frames. A bus system used internally in PUC is extended to serve one or two complete MAS frames, and is designed to accommodate additional units in the future. Each PUC controller provides two extended internal buses (EIBS); all MAS units connect to one of the buses from each PUC controller. Each bus contains a 24-bit, parallel two-way data field. Data flow on each bus is under control of its associated PUC controller. Source and destination fields govern the transfer of information in either direction between internal PUC and MAS registers. Additional leads are provided for handshaking and error-control purposes.

## III. EQUIPMENT DESIGN

Throughout the mass announcement subsystem, the recently introduced *BELLPAC** packaging system technology is used.[4] The major subsystem components are the PUC frame, the MAS frame, and the disk systems. Figure 2 shows a photograph of the complete subsystem. Both frames use *BELLPAC* packaging system technology, and are 39 inches wide and seven feet high; the PUC frame is 12 inches deep (usual for No. 4 ESS), while the MAS frame depth is 18 inches. The MAS frame depth reflects use of circuit packs also used in the 3B Processor system.

The PUC frame houses one duplicated peripheral controller unit, a duplicated PUB interface, and associated power equipment. A vertical cabling trough divides controllers 0 and 1; the controllers are generally mirror images. The two PUB interfaces are located above the controller units, and principally contain the cable drivers and receivers required to interface to the No. 4 ESS processor. Power supply equipment for each controller unit is located in the lower part of the PUC frame; +140 V input power is converted to +5 and −5.2 V for use within the frame, and +24 V input power is used directly. Power for the PUB interfaces is separate and is derived from converters located in the PUB units. Electronic sequencing, regulation, and overload control is provided on circuit packs located both in controller and PUB units.

The MAS complex contains a single-bay frame and two 80-Mbyte moving-head disk drives (Fig. 2). The two disk drives are located on each side and adjacent to the MAS frame. The frame is equipped with two identical MAUs and associated power equipment. Each MAU is associated with one disk and consists of a controller and circuits interfacing to the PUC, the disks, and the No. 4 ESS switching network.

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* *BELLPAC* is a trademark of Western Electric.

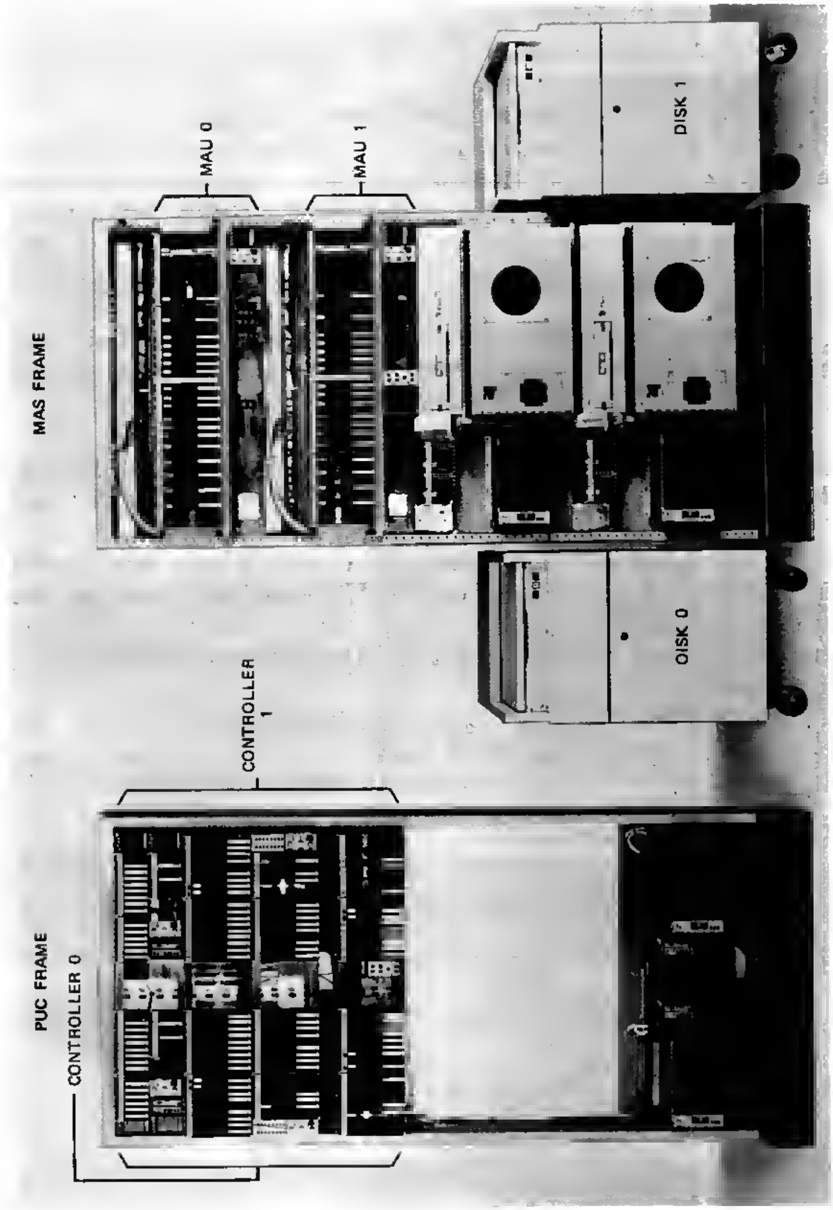


Fig. 2—Mass announcement subsystem frame complex.

The lower half of the MAS frame is used to house the power equipment. To provide autonomous operation of the two MAUs and the associated disk drives, duplicate power feeders of +140 V, +24 V, −48 V dc and 208 V single-phase ac are cabled to the frame from their respective No. 4 ESS office power plants and from the office power

service circuit. The +140 V is converted to +5 V, −5 V, and +12 V dc for use by the MAUs. The −48 V is inverted to 208-V ac for use by the disk drives whenever commercial ac or central office essential ac is interrupted or falls outside the drive's operating limits.

The circuit packs in both the PUC and MAS frames use both Schottky and low-power Schottky transistor-transistor logic, and high-speed emitter-coupled logic contained in dual in-line packages (DIPs). Three different sizes of circuit packs are used; the sizes vary from 4 by 9 in. to 8 by 13 in. Connector pinouts available on these packs number 100 or 200 pins.

The circuit pack technologies used are the double-sided rigid board and the multilayer board with both external and internal power and ground planes. Both types are nominally 0.0625-in. thick.

The double-sided rigid board is an epoxy-glass board with etched copper-printed wiring on both sides. Path widths range from 0.006 in. to 0.050 in., and plated-through holes of 0.020 in. are used. This board is primarily used for low-density circuitry.

The multilayer boards are used in four- and six-layer versions and are used for high DIP packing densities. The four-layer boards use the two external layers for distributing power and ground and for the connector fanout patterns. The two internal layers are assigned to signal routing.

In the six-layer versions, power and ground planes occupy the innermost internal layers, which improves electrical characteristics. Several voltage levels can be provided through segmentation. The two

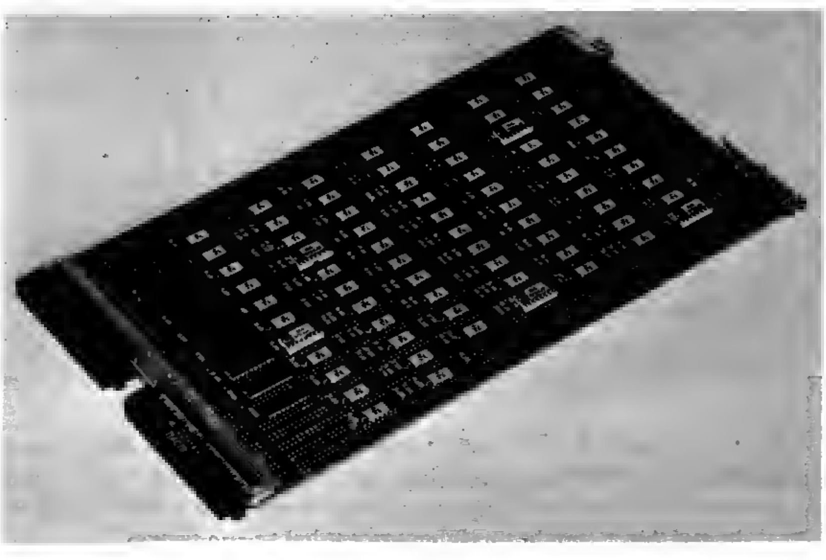

Fig. 3—*BELLPAC*™ packaging system technology TN circuit pack.

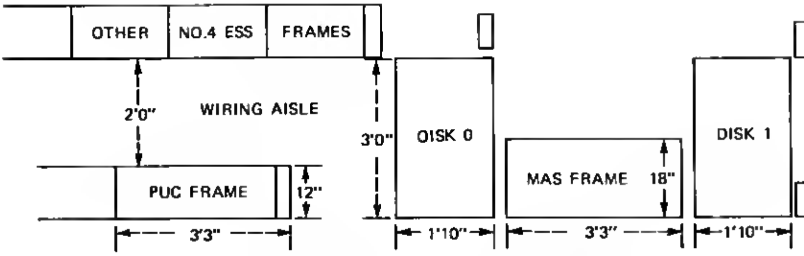


Fig. 4—Mass Announcement System floor plan.

external layers are generally used only for soldering pads and for connector fanout patterns, but can also be used for signal routing, if necessary. The remaining two internal layers are for signal routing. Signal paths on the multilayer boards can be as large as 0.025-in. wide and can be decreased to 0.008 in. where two paths pass between DIP terminals or plated-through holes.

A six-layer 8- by 13-in. circuit pack is shown in Fig. 3. Both power supply filtering and a large number of decoupling capacitors are used on this pack. These capacitors are judiciously placed to minimize noise.

A maximum of eight MAS complexes, each consisting of one MAS frame and two disk drives, may be installed in a No. 4 ESS office. However, to meet reliability objectives, a maximum of only two MAS complexes may be connected to a PUC frame.

A typical central office floor plan for one mass announcement subsystem is shown in Fig. 4. Because of the disk size, the MAS complex consumes the space normally allotted to two frame lineups. The disks also provide a convenient break in the frame lineup so a MAS frame with a depth of 18 in. can be used; most No. 4 ESS frames are 12 in. deep. The PUC and MAS frames are placed in the same lineup to keep the interconnecting cables as short as possible.

## IV. PERIPHERAL UNIT CONTROL CIRCUITS

The PUC frame provides a control interface between the No. 4 ESS processor (1A Processor Common Control) and new equipment that must be controlled by the processor. The mass announcement subsystem frame is the first user of the PUC, but the PUC has been designed so that future services can be added easily, with only PUC microprocessor firmware changes required. This eliminates the need to develop a new processor interface for each new hardware system, and saves on the cost and time required to add services to the No. 4 ESS.

Much of the PUC circuitry is similar to the controller of the DIF, which is discussed separately.[3] We review briefly the common portions.

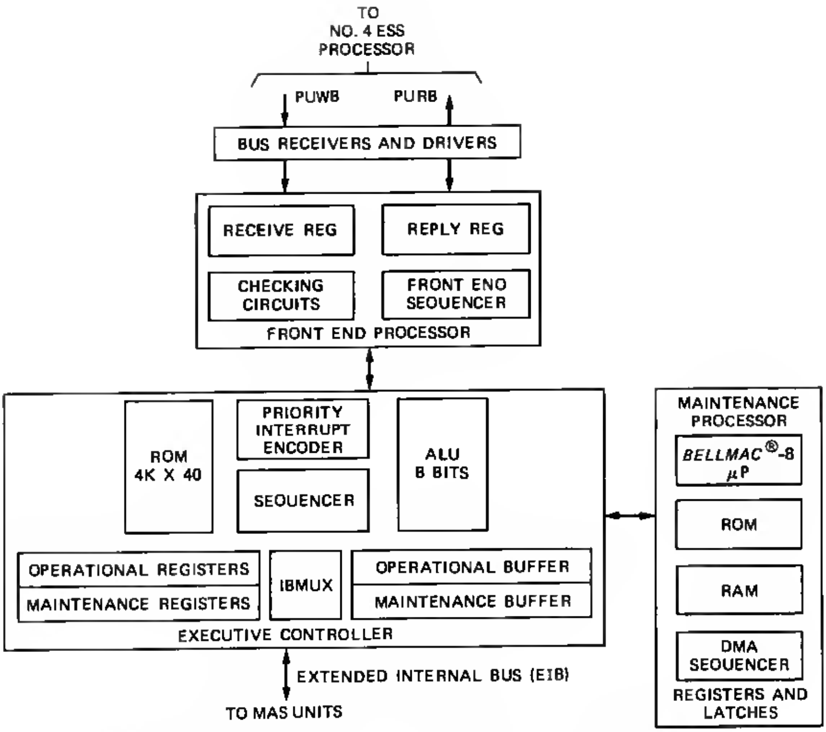


Fig. 5—Peripheral Unit Control frame controller block diagram.

The main unique features of the Peripheral Unit Control circuits include the extended internal bus which connects to the mass announcement frame, and the microprocessor programs or "firmware" that govern the controller's operation.

Each PUC controller centers about an executive controller (Fig. 5), a high-speed bipolar-technology microprocessor which provides processing functions and controls data transfer operations on an internal bus. The executive controller has access to registers and buffer memory, and controls interfaces to the PUB and mass announcement frame. A second maintenance processor can be used for background tasks.

### *4.1 No. 4 ESS processor interface*

The duplicated PUB provides the data and control path between the No. 4 ESS processor and the PUC frame. Figure 1 shows the interface between the No. 4 ESS processor and the PUC frame. The PUB interface provides a fully duplicated communication path between the processor and the PUC frame. Each bus consists of four groups: the enable address bus, the write bus, the reply bus, and the control bus. The enable address and write buses (PUWB) convey instructions from the

processor to the PUC, while data from the PUC is sent to the processor via the reply bus (PURB). Control and maintenance information is transmitted to and from the PUC over tbe control bus. Each of the duplicated PUC controllers has full two-way access to both buses; bus access routing is controlled by the No. 4 ESS processor througb flip flops in the PUC.

Circuits that provide access logic to the bus consist of a receiving register, a reply register, a sequencer, and checking circuits. Orders from the processor to the PUC are sent over the PUWB. The order is latched in a receiving register, and checked for validity and for the correct address code. For valid orders, the hardware generates a high-priority interrupt to the executive controller, which then processes tbe order. When processing is complete, the results appear in the reply register, usually within 20 μs. The bus access hardware then gates the reply data onto the peripheral unit reply bus. The bus access logic removes significant real-time overhead from the executive controller.

### 4.2 Executive controller

The executive controller is a microprogrammed bit-sliced processor with a basic cycle rate of 4 MHz. It accepts interrupts from three external sources: from the No. 4 ESS processor, from the MAUS, and from the maintenance processor located within each PUC controller. An interrupt request points to a starting address in the firmware microprogram, a set of routines that route data between different registers and memory locations. The firmware microprogram is contained in 4096 words of read-only memory (ROM); each word is 40 bits wide, of which eight bits are used for parity checking. Processor hardware consists of ROM, sequencer, interrupt control, and arithmetic and logic circuits.

Addressing for tbe microprogram ROM is by sequencer circuits, which provide for conditional program branching. External interrupts are handled by a 16-level priority interrupt controller, which passes a starting address to the processor when an interrupt is received, and an 8-bit-wide arithmetic and logic unit provides computational power. Certain critical circuits (arithmetic unit, sequencer, and interrupt control) are duplicated within each controller; matchers between the duplicated circuits provide improved fault detection.

### 4.3 Registers and buffer memory

Each controller in the PUC frame contains a set of internal special-purpose operational and maintenance registers. Operational registers include a status register, reflecting critical configuration and data routing states; receiving and reply registers for incoming and outgoing orders from the No. 4 ESS processor; and a cutoff register used to

isolate MAS units from the PUC. Maintenance registers include error-source registers (ESRS), or error indicators, for hardware failures; an exercise register that creates abnormal conditions to verify the operation of error-detection circuits; and a pest register for disabling individual error indications.

The PUC controller has access to a 24-bit, 256-word random-access memory (RAM). This RAM is logically divided into operational and maintenance buffers, and is principally used as intermediate storage for MAS operational and maintenance reports to be forwarded to the No. 4 ESS processor.

### *4.4 Internal bus*

Data transfer within each PUC controller is via a 24-bit data bus; in addition, 6-bit code fields are provided to select the source and destination of each data transfer. Each possible source register is assigned to one port of a 16-port multiplexer; the source code selects the appropriate register and port. The output of the multiplexer is routed to all possible destination registers; the proper register receives the data in response to the appropriate destination code.

The internal PUC data bus is extended outside the frame to serve MAS and other circuits that may be provided in the future. One bidirectional data bus serves all MAS units connected to each PUC controller. Tristate, dc-coupled cable drivers are provided at each unit; cutoff leads are provided to disable MAS units suspected to be faulty. Additional control leads are provided for handshaking and synchronization of data transfers between PUC and MAS.

### *4.5 Maintenance processor*

A maintenance processor is used for localized diagnostic and fault recovery within the controller. This is a *BELLMAC*-8 single-chip, bus-structured, general-purpose microprocessor, with 60K words of ROM program and 4K of RAM. The maintenance processor is capable of interrupting the executive controller and simulating No. 4 ESS processor orders. Fast, direct access by the No. 4 ESS processor to the maintenance processor RAM is provided. Maintenance processor programs include an operating system, bootstrap routines, maintenance processor diagnostics, and application programs used to initialize the PUC frame.

### *4.6 Peripheral Unit Control programs*

The PUC processor complex is programmed to handle operational and maintenance instructions from the central control and units on the extended bus. The executive controller programs that handle these jobs are organized as a hierarchy of tasks entered from a control

program that services interrupts and controls job scheduling. Since the controller is an interrupt-driven processor, the program services interrupts from the No. 4 ESS processor and MAS interfaces, plus maintenance interrupts, such as errors and real-time clock interrupts, which initiate exercise and audit routines.

### 4.7 No. 4 ESS processor order-handling programs

Processing No. 4 ESS processor orders that have been detected and validated by bus access circuitry is a principal function of the executive controller. The hardware first generates an interrupt request; if an autonomous or background task is running, the task is interrupted at an appropriate point and the incoming order is processed. The opcode part of the order is used as an index to branch to the program. The remaining parts of the order are used as data or address information to access specific registers or memory, or initiate multiple-operation macro functions. For a simple read register order, the task routine moves data from a register selected by the program into the peripheral bus reply register. Similarly, for a write order, data moves from the peripheral bus receive register to a destination register. When the write order is completed, the reply register is loaded with an order to return an all-seems-well (ASW) acknowledgment to the No. 4 ESS processor. Controller hardware takes over once the reply register is accessed; a hardware sequencer is used to return ASW and data to the No. 4 ESS processor in conformance with bus timing requirements. Execution then returns to the program that had been interrupted, or to an idle routine if no jobs were active when the No. 4 ESS processor order interrupt occurred.

### 4.8 Mass Announcement System order-processing programs

A unit on the PUC extended bus, such as MAS, initiates communication with the No. 4 ESS processor by loading reports in buffers in the PUC executive controller RAM. Processor orders periodically unload these reports. The reports may be responses to macro tasks previously initiated by the processor, or the unit may initiate reports autonomously due to operational or maintenance conditions. To load a report in the PUC, the unit loads the report type and data in its reply register and signals on a common party-line interrupt request lead. The PUC interrupt-handler routine polls the units on the bus to determine which units require service, and then reads the report data. A task-dispenser routine services each unit that responded by examining the report-type field and branching to a task designed to handle that data. When a task has been handled successfully the controller program resets the unit's reply register and interrupt request. If a report cannot be

handled because a buffer is full, the interrupt request for the unit remains set, and a retry is attempted later.

In the reverse direction, the PUC initiates communication with a peripheral unit such as MAS by checking the receiving register on the communication register pack. If the upper byte of the register is nonzero, an earlier order has not yet been acknowledged by MAS, which services the receiving register every 250 $\mu$s. In this case, the order will be reattempted later. If the upper byte is zero, then the PUC sends the order to the receiving register and places a nonzero value in the upper byte of the register. When the MAS controller next checks the upper byte, it unloads the receiving register, and zeros the upper byte.

Two buffers are assigned in PUC for communication from MAS to the No. 4 ESS processor. Operational reports are loaded in a low-priority buffer dedicated to handling single-word reports. (A high-priority buffer, used in certain other No. 4 ESS frames, is not used in PUC/MAS.) A maintenance buffer sends multiword diagnostic raw data and echo reports, which acknowledge all orders sent to MAS. The PUC performs protocol checks on reports received from MAS, and reports irregularities to the No. 4 ESS processor.

### 4.9 Exercise and sanity programs

To aid in the rapid detection of faults, an exercise program is included in the PUC. This program is entered every 10 ms by an interrupt request generated by the controller clock. The program tests all of the controller logical and arithmetic operations. The ability to access most of the registers is tested by read instructions. The test does not destroy register data and is segmented so it can be interrupted by processor orders within 3 $\mu$s. Hardware error detectors are used to verify proper operation. If a failure occurs, ESR bits are set that alert the processor by a peripheral bus maintenance interrupt. The 10-ms interrupt is also used to make a maintenance buffer sanity check; should a multiword report being loaded in the buffer not be completed in a reasonable time, the report is closed so that new reports may be loaded.

### 4.10 Peripheral Unit Control frame summary

In summary, the PUC contains hardware and microprocessor software to provide an interface between the mass announcement frame and the No. 4 ESS processor. The Peripheral Unit Control frame is designed with flexible interconnections so that equipment to provide new features may be easily added to the No. 4 ESS hardware community in the future.

## V. MASS ANNOUNCEMENT SYSTEM FRAME

The MAS frame contains two mass announcement units, each associated with a disk storage system. The units connect to the extended

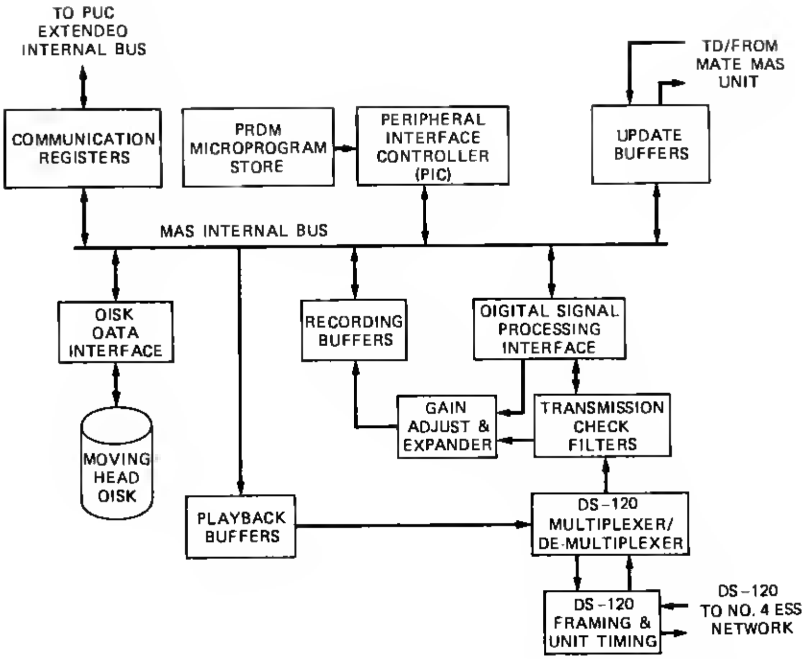


Fig. 6—Mass Announcement System unit block diagram.

internal bus of the PUC for control purposes, and via 120-channel DS-120 links to the switching and permuting circuits of a TSI frame in the No. 4 ESS switching network for recording and playback of recorded announcement signals. Figure 6 contains a block diagram of the major components of a mass announcement unit.

New announcements are placed on the disk by allocating appropriate sectors and designating them as "standby," i.e., not currently playing back. The announcement is then recorded on one disk over a DS-120 link channel via a recording buffer. Coordinating messages are sent from the No. 4 ESS processor to both disks, and the announcement is transferred via an update buffer and a dedicated bus to produce a duplicate copy on the disk of the second announcement unit. Later, under processor control, both MAS units are instructed to change the announcement status from "standby" to "active," and actual playback begins.

### 5.1 Playback system

Each MAS unit provides announcement playback of 30-s message segments which are read from the disk. Any segment may be assigned to any of the DS-120 link channels dedicated to playback, and segments may be concatenated. Since part of a segment may be silent, the

system has the ability to play messages varying from a few seconds to 5 min in length. Each unit can provide up to 29.5 min total storage of announcements ready for playback.

Although the two units generally store the same announcements, the units are duplicates only in a limited sense. Each MAS unit is essentially a simplex unit playing back announcements independently of the other unit but skewed in time so that when one unit begins the playback of a new cycle of 30-s announcement segments, its mate unit is at the midpoint of its 30-s segment cycle. The No. 4 ESS system connects callers to the announcement unit which first reaches the beginning of the required announcement; the skewing reduces the average waiting time to 7.5 s (Fig. 7).

Each 30-s message segment is stored on the disk units in the 64 kbit/s serial PCM data format used on digital transmission facilities and within the No. 4 ESS network. The storage medium used is an 80-Mbyte moving-head disk system. Each message segment is allocated a three-dimensional portion of the disk storage called a "sector," which

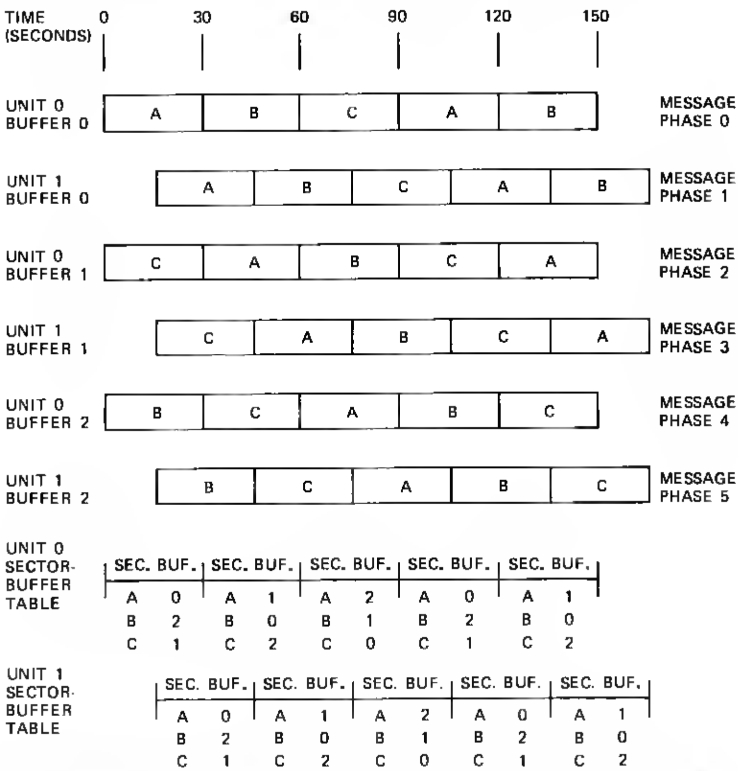


Fig. 7—Message Phase construction. Construction of the six phases of a 90-second message stored on disk sectors A, B, and C.

comprises all the accessible data within an angular portion of the disk. A small section of every active announcement segment is accessed by the disk heads upon each disk revolution.

In operation, the MAS unit reads short pieces of each announcement from the disk into individual playback buffers; all active announcements are served sequentially. The buffers are emptied at a slower rate into the appropriate time slots of the DS-120 link, one 8-bit PCM sample being read out per announcement each 125 $\mu$s.

Data read off the disk are converted from serial to parallel form and error correction is performed based on cyclic codes. Parity is generated, and, after an intermediate buffering stage needed because of speed differences, the data are transferred to the playback buffer for delivery to the DS-120 link.

Each of the 64 playback buffers is permanently assigned to one of the 64 even-numbered DS-120 channels 0 to 126. Of these channels/buffers, four are dedicated to maintenance activity and up to 14 others may be optionally designated as monitor channels. Of the remaining 64 channels, 14 are permanently assigned as recording channels, two are maintenance recording channels, two are loop-back channels to the TSI, and the rest are not used.

### *5.2 Recording and updating system*

Announcements may be recorded, activated, and deactivated via dedicated transmission facilities in the telephone network by a centralized administration center (Fig. 8). This function is important in the offering of coordinated, nationwide mass announcement services. The administration center accepts and stores announcement messages from sponsoring telephone companies and commercial advertising sponsors, and handles the distribution of these announcements to MAS frames in No. 4 ESS offices.

Since the recording of announcements on the MAS disk may involve long distances, transmission checks are done at the MAS end. The voice signal is amplitude-compressed at the transmitting end and a pilot tone at 2150 Hz is added so that levels can be monitored. Within the telephone network the signal is converted to PCM digital format, with additional compression according to the $\mu = 255$ law quantization companding standard.

At the MAS end, the PCM data arrive on one of the assigned recording channels of the incoming DS-120 link and are routed through digital signal processing circuitry which first converts both the voice data and the pilot tone back to linear PCM. A noise check on the transmission link is performed before and after the announcement data are received. Digital filtering is used to separate the tone from the voice data, and to adjust the signal level based on the tone level. The signal is also

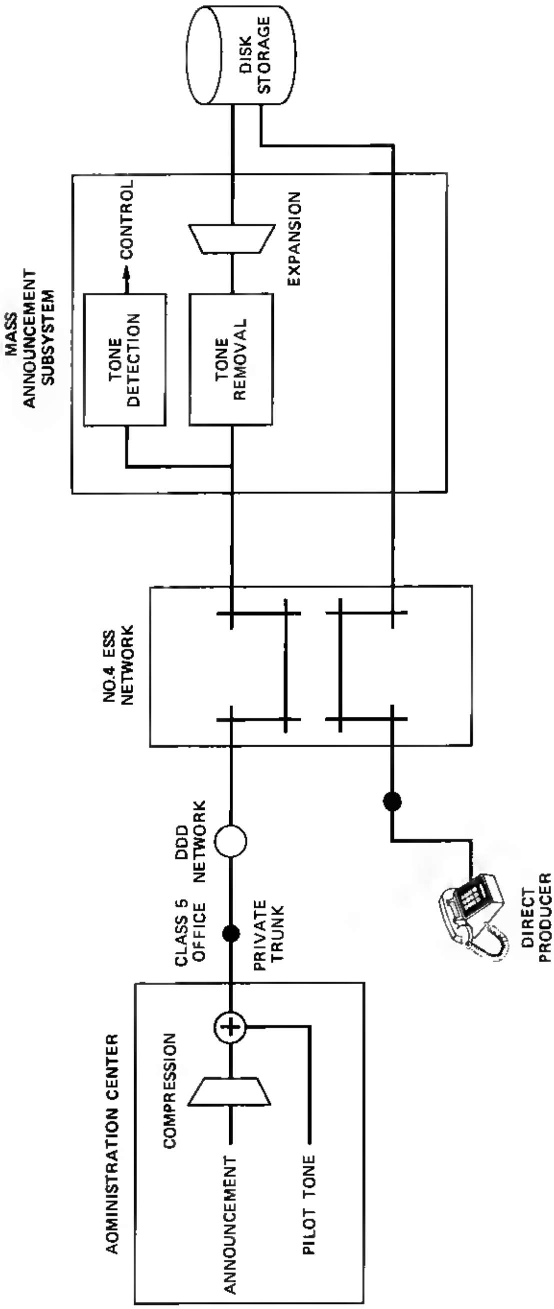


Fig. 8—Direct Distance Dialing network interface.

expanded to remove the compression which was inserted at the administration center. If the tone level is not within specified limits, the network connection is rejected and a retry is requested. The PCM data are finally reconverted to $\mu = 255$ format, changed to parallel form, and delivered to a recording buffer. The data are then written into the assigned disk locations.

Once an announcement has been recorded onto the disk of one MAS unit, a transfer or update of the announcement is scheduled for the other MAS unit. There are dedicated bus paths for updating in either direction between units, with update buffering capable of storing about 16 s of digitized voice at each unit. At the appropriate time, data are transferred in blocks from the originating MAS unit disk through the update buffer to the destination MAS unit disk. This transfer allows the system to provide duplicated announcements with skewed phasing.

Provision has also been made in MAS for local recording of announcements directly, without the assistance of an administrative center. This feature is invoked by placing a telephone call to a special telephone number which results in a connection to an appropriate No. 4 ESS equipped with MAS. A tone is played back to the producer from the recording buffer; this indicates that the desired recorded message should begin. Digital signal processing does not occur in this mode; message quality is confirmed when No. 4 ESS calls back the announcement producer and plays the recorded announcement. The producer decides whether sound quality is acceptable and either approves the recording or repeats the entire process.

### *5.3 Controller hardware*

Central to the operation of MAS is a microprogrammed controller using bit-sliced architecture. This Peripheral Interface Controller (PIC) performs the basic function of data transfer between the moving-head disk and the playback and recording buffers. It also controls execution of orders from the No. 4 ESS processor via the PUC and generates replies. Typical actions include reporting on system and announcement status, updating announcements from one unit to the other, and performing operational and on-request diagnostics.

The PIC is a 16-bit microprocessor-based controller designed using Advanced Micro Devices, Inc., 2900 series bit-sliced integrated circuits. It is capable of a memory-to-memory data move operation in 183 ns. The processor also has 4096 words of 18-bit data RAM, eight priority-encoded interrupts, a sanity timer, a scratch register, and 17 general purpose registers in the arithmetic and logic unit.

The program for the processor is stored in programmable read-only memory (PROM) on three circuit packs. Each instruction is 40 bits

wide, including four parity bits. A total of 4096 instructions can be stored on a single program store circuit pack.

The PIC performs 40-bit program instructions resident in its 12K of PROM in a pipelined fashion for purposes of speed and efficiency; while the present instruction is being executed the next is being fetched by the PIC's sequencer. Each instruction's speed of execution may be set to 183 ns or 366 ns by the program itself. Data is transferred between ports on an internal bus by specifying source and destination fields within program instructions.

The No. 4 ESS processor communicates with the MAS unit via tbe PUC's extended internal bus. This duplicated 24-data-bit bus is routed sequentially from one MAS to the next, and enables either PUC controller to communicate with eitber MAS unit.

Orders are sent from the No. 4 ESS processor via the PUC over the extended bus to the MAS register, and reports of MAS activity leave the unit from the reply register. Each MAU interfaces with both buses of the duplicated EIB. The interface consists of two bus driver and receiver circuit packs and a communications register pack. Each bus driver-receiver pack includes in its circuitry an interrupt identification code generator and a bus source and destination decoder. An MAS frame and unit identification code is wired into these two circuits during office installation.

The PUC may monitor the general health of a MAS unit by reading the MAS ESR, part of the communications register. The lowest three bits (EIB parity error, invalid controller activity, and communications register interwrite error) indicate communications failure between MAS and PUC, and result in a peripheral unit failure (F-level) interrupt in the No. 4 ESS processor. The remaining 21 ESR bits indicate problems of less severe nature and, when set, they generate a request to the PUC for service. Three of these bits are directly wired in from the appropriate circuit packs to indicate PIC program memory parity failures, program sanity time-outs, and clock errors. The remaining bits are set by program tests, and include errors such as playback buffer errors, disk control errors, and DS-120 framing and timing errors. The uppermost five ESR bits provide the No. 4 ESS processor with information on ASW failure errors which occur when MAS cannot successfully complete an order from the No. 4 ESS processor. The first bit indicates ASW failure; the remaining four bits form a code that indicates the specific problem that the PIC had in handling the order.

The PUC may place the MAS unit in a particular state by writing the unit's status register, which is bit-writable by the PUC and readable by both the PUC and the PIC. The PUC can place the MAS unit in a maintenance mode or a simplex mode (mate unit out-of-service) by setting appropriate status register bits. An initialization bit forces the

PIC program address to zero and halts execution. Other status bits can be set to mask ESR summaries to the PIC and interrupt requests to the PUC.

### 5.4 Disk control programs and disk organization

The PIC program's principal function is to act as a disk controller; the majority of the processing power is spent transferring data between the disk and the buffers. Other functions of the program have been designed to fit into the structure determined by the disk accessing tasks.

Efficient playback of announcements from the disks is facilitated by a regular organization of the announcement storage locations on the disk. Since all announcements begin in synchronism, the exact time in each cycle when a given section of an announcement must be read is predictable. The PCM data for all announcements are interleaved so as to minimize the travel of the moving read/write magnetic heads.

Announcement storage is provided on a five-platter removable disk pack controlled by an 80-Mbyte moving-head random-access disk drive. The top and bottom platters serve only to protect the three operational platters. The three operational platters provide five data faces and one clock/servo face. The five data faces are divided into

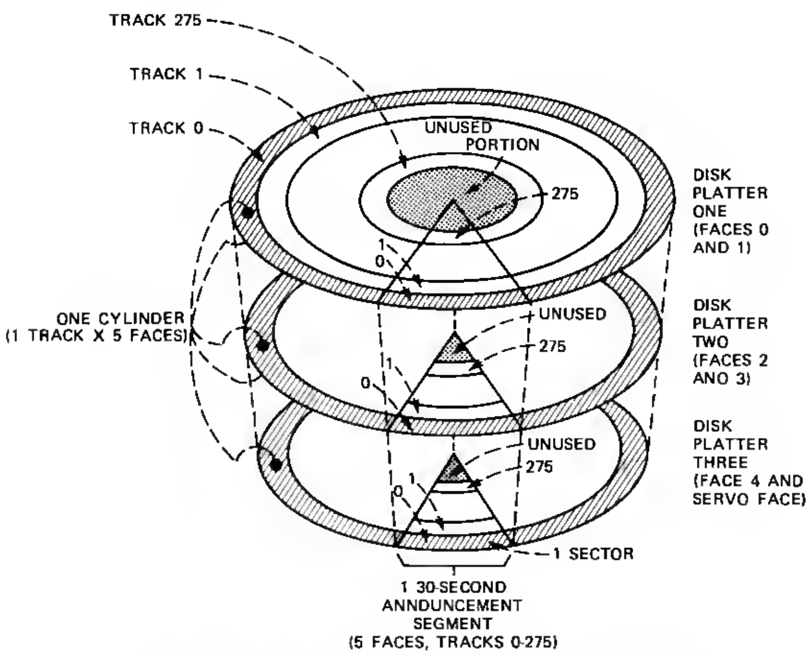


Fig. 9—Disk storage allocation for a 30-second announcement.

aligned annular tracks; 276 tracks on each face are used operationally. Each track is further divided into 86 angular sectors, with the sector boundaries aligned over all tracks and faces. The sets of corresponding tracks across all data faces form 276 cylinders. Each 30-s announcement segment is concentrated within one angular sector, but spread across the tracks and faces within that sector (Fig. 9).

The disk is scanned in 30-s cycles. This is done first by reading all active announcement sectors on the outermost track of each data face in succession to complete the scan of the outermost cylinder, cylinder 0. A small portion of each announcement segment has then been read. Then the heads are moved to cylinder 2; the process is repeated for all even cylinders to cylinder 274. Starting from cylinder 275, the direction of the head motion is reversed to scan the odd-numbered cylinders while the heads return to the outer rim of the disk. The complete process requires 30 s.

### 5.5 Task scheduling

In addition to controlling disk-head movement and disk-data transfer, the disk-data handler program functions as an executive controller to schedule other tasks. These tasks are scheduled for intervals when disk-data transfer must be suspended for various reasons. During disk-data transfers, the controller is fully occupied with this task.

During the time that the heads are moving from one cylinder to the next or "seeking" the next cylinder, the controller is free to execute other tasks. These tasks are called "seek jobs" and are limited to 9.6 ms in duration. In addition, since the disk-transfer rate into the buffers exceeds the rate at which the buffers are unloaded, the disk accessing must be suspended periodically or "slipped" so that the buffers do not overflow. These suspensions can occur after any track has been scanned, except when a seek is pending. During the time that the disk access is suspended, approximately 9.6 ms, the controller is free to execute other tasks, called "slip tasks." Slip tasks are reserved for self-testing, which are covered later under overall PUC/MAS maintenance. Tasks less than 100-$\mu$s long can be executed during idle sectors, which contain no active announcement data. Finally, a period of about 10 $\mu$s is available at the beginning of each sector during which no program action is necessary to maintain data flow (Fig. 10).

### 5.6 Operational and maintenance tasks

Program tasks in MAS that handle communication with the PUC require only a short amount of time but must be executed frequently. These actions are covered by a "preamble job" executed in a 10-$\mu$s period near the beginning of each sector. This task is also scheduled at approximately 250-$\mu$s intervals by long-duration tasks, such as seek or

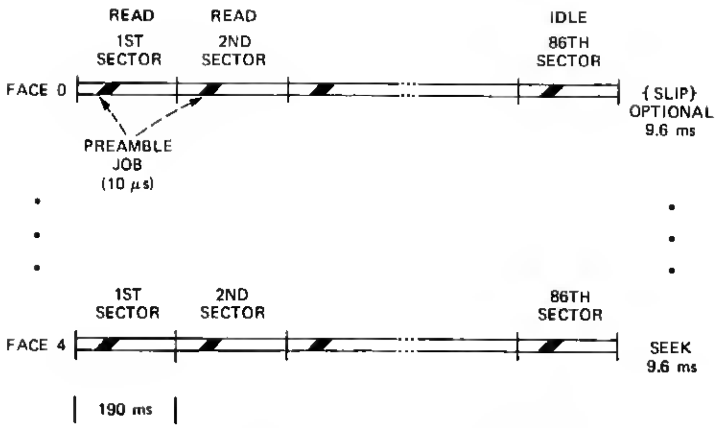


Fig. 10—Typical program flow for one cylinder.

slip jobs. The preamble job unloads the MAS unit receiving register into a queue maintained in PIC RAM, and loads the reply register from a second queue in RAM. Operational and maintenance tasks process the received orders and generate the replies.

All operational tasks are scheduled during seek or idle sector intervals. For example, during every fourth seek the seek task dispenser schedules a message-timing task. This task performs announcement phasing and concatenation of 30-s segments during recording and playback. The message-timing task also processes information in the announcement status, buffer allocation, starting point and sector allocation tables to update the sector buffer table, which governs disk data transfer. In addition, a unique task is selected for each seek interval in the 30-s cycle, and additional "once-per-cylinder" tasks are executed during each seek interval.

Self-test tasks are performed during slip intervals. We cover self-testing later along with overall maintenance of the PUC/MAS subsystem.

Certain short tasks are performed during the 100-μs intervals during idle sectors. Two idle sectors per disk revolution are reserved for scanning the tone and noise detectors of the digital signal processing circuits used in recording. Data are collected which determine the average level and noise values for each recording channel. This is used to provide automatic gain control; should the signal level or noise become unacceptable, the program aborts the recording.

During other idle sectors, the No. 4 ESS processor order-execution routine is called. This routine leads an order out of the receiving register queue and passes control to an order routine determined by a data field in the order. Typical orders involve allocation or deallocation

of sectors and buffers, recording, monitoring, and playback of announcements, and duplication of sectors. These orders change the state of the message tables, thus, allowing the message timing and control routines to properly execute the desired action. Other processor orders can be used to read or write PIC RAM locations, diagnose particular circuits, and start or stop the unit.

### 5.7 Update tasks

Duplication of announcements between MAS units via the update buffer is another task executed by tbe PIC. This transfer is performed on a per-sector basis. If a sector is to be updated, a No. 4 ESS processor order alerts the unit that acts as the source. During the cylinder 0 task, the sector buffer table is altered to begin to load the given sector into the update buffer. The processor then instructs the receiving MAS unit to set up its sector buffer table to unload the update buffer into the correct sector on the disk. The receiving unit begins to transfer data from the buffer to its disk 15 s after the source unit begins filling the buffer. Since each unit has an update buffer, duplication can occur in both directions at once.

If one unit is taken out of service, its disk must be updated before it can be restored to service. This maintenance update is initiated by processor order. In this process, the update buffer is used to transfer all of the useful data on the in-service unit to the out-of-service unit. The process begins when the in-service unit accesses cylinder 0. At this time, the in-service unit writes all of its message-timing tables into the update buffer. This data is used by the receiving unit to interpret the announcement data which is written to its disk from the other unit. The in-service disk then begins loading disk data into the update buffer one cylinder at a time; the receiving unit then empties the buffer. The cycle repeats until the update is complete; this requires about 60 s.

## VI. MAINTENANCE FEATURES

Dependability and maintainability are important considerations in the design of the PUC and MAS bardware subsystem. These considerations are in line with the high reliability and maintenance objectives of the entire No. 4 ESS switching system. The PUC/MAS maintenance plan is integrated into that of No. 4 ESS. Dependability is achieved by ensuring rapid detection of failures and by providing hardware redundancy that enables acceptable service to continue in the presence of faults. Maintainability requires that maintenance personnel have available automated diagnostic tools to permit rapid isolation and repair of failures.

### 6.1 Maintenance architecture

Differences in maintenance philosophy exist between the PUC and MAS frames. The Peripheral Unit Control circuit is an interfacing circuit on which several MAS frames and possibly other future services rely. A PUC failure that results in loss of service on all of the connecting equipment is intolerable. To avoid this, the PUC is fully duplicated; its two simplex halves normally run in synchronism, executing identical tasks. Each is fully capable of providing full service should the other fail. The synchronization of the two halves complicates the hardware design but eases the job of fault detection, as matching between the two halves is possible. The MAS frame also consists of two identical halves, or units. As has been noted, however, the two MAS units do not operate in synchronism; they perform similar tasks but at different times. Matching between units is impossible; to aid in fault detection, regular self-testing routines are executed. In the event of failure of one unit, service continues, but longer waiting times are experienced by callers.

### 6.2 Fault detection

Maintenance actions begin wi'h error detection. In the PUC, matching between controllers, self-checking logic, and internal duplication within controllers are employed to achieve a high level of on-line immediate detection of transient and permanent errors. Protection against data transmission errors is provided within all the controller data paths using coding techniques, loop around, and hardware checkers. All data in memory (RAM/ROM) are coded and checked. Critical portions of the hardware processors (arithmetic and logic unit, maintenance microprocessor, and internal bus multiplexer) are duplicated and matched. A local ESR (hardware monitor) is provided for each major functional unit to allow high resolution of error location. Exercise and pest registers are employed to control and test the hardware monitors. Errors in the controller are summarized in a primary ESR, which, when set, causes a maintenance interrupt to the No. 4 ESS processor. The processor calls fault recovery programs for appropriate actions.

The MAS units use similar fault detection techniques to those used in PUC, except that matching between units is not possible and additional self-testing is required. Hardware faults in MAS result in bits being set on the MAS unit's ESR, which, in turn, immediately sets a PUC ESR bit.

### 6.3 Mass Announcamant System self-test

Since the MAS unit does not run in step with its mate unit, matching cannot be used for operational error detection. This requires that a

sufficient number of audits, checks, and tests must be written into the operational firmware program along with dedicated self-test hardware to detect faults during normal operation of the unit. Parity is used on RAM in the unit to aid in error detection. Also, additional hardware access and looping capability has been provided to allow the firmware to more easily test the various hardware modules.

The firmware self-test tasks are executed during seeks, slips, and certain dedicated idle sectors. Some disk sectors are not used for operational purposes; this allows execution of various miscellaneous tasks to provide self-testing. One such task is a scan of error counters which are decremented by certain operational and data handler routines when an error is found. These counters are loaded with some initial value; a negative count causes an error to be reported. This technique reduces the effect of transient errors and also reduces the load on real-time critical processes. Peripheral Interface Controller RAM is checked by performing access tests on RAM data and address registers, and parity and hash checks over software protected areas. Access tests are also done on all playback and record buffer registers. Maintenance buffers are used to do partial memory testing. The disk and disk hardware is checked by accessing a dedicated idle sector; random data is continuously written, read, and verified on this sector, and every track of that sector is processed in a 60-s period. Disk data itself is protected by a powerful error detecting and correcting cyclic redundancy check code, capable of correcting burst errors of up to 11 bits in length.

A playback and recording loop test is also performed. Data from the playback buffer is looped to a recording buffer and then verified. This loop feature is also used to test the digital signal processing circuits. Various dc levels and tones are looped through these circuits to ensure that the proper filtering action is taken. Since the signal-processing circuits are used in a time-multiplexed fashion, the circuits can be fully tested by using a maintenance time slot at the same time other time slots are being used operationally.

All slip tasks are dedicated to self-test. The slip task dispenser monitors the DS-120 framing circuit and controls update buffer testing. The tests executed include an update buffer register test, a march test on the memory fabric, and a check of the cross-unit update access circuits. Update tests are not executed if update work is in progress.

### *6.4 Diagnostic software*

Diagnostic software is available for both PUC and MAS. It can be used under control of maintenance personnel as an aid in fault isolation. Certain portions or "phases" are invoked automatically before out-of-service hardware can be restored to service. Diagnostic software in

PUC/MAS is, in some cases, executed by the No. 4 ESS processor, and consists of a series of tests which send orders to PUC/MAS and evaluate responses. Other portions are initiated by processor orders but are executed by programs in PUC or MAS.

The PUC is a multiprocessor controller employing a hardwired processor, bit-sliced microprocessor, and a maintenance microprocessor. The diagnostic programs have been developed to suit this multiprocessor structure. The diagnostic software contains No. 4 ESS processor resident diagnostic programs that test the PUC front-end processor logic, power, clocks, the interface between the PUC and the No. 4 ESS processor, and the synchronization between the duplicate PUC controllers; and executive controller resident diagnostic routines that are invoked by No. 4 ESS processor orders. These routines perform tests on the arithmetic and logic unit, the priority interrupt encoder, the microsequencer, and in general on the logic that is directly under control of the executive controller ROM. These test results are passed to the No. 4 ESS processor diagnostic programs for analysis and decisions. Diagnostics are also resident in the PUC maintenance processor. These are executed by the maintenance processor under macro commands from the No. 4 ESS processor. These programs perform localized self-testing on the MP hardware, and also interact with the executive controller to diagnose its hardware. Maintenance processor test results are passed to the No. 4 ESS processor via the maintenance buffer.

The MAS diagnostic is composed, like the PUC diagnostic, of a No. 4 ESS processor resident part and a firmware part. The processor resident part provides all necessary interfaces between the PUC unit and the rest of the ESS system. The diagnostic first checks power and the PUC/MAS interface circuits; these phases are processor resident. The MAS firmware part of the diagnostic contains some tests which run only on specific processor orders. Other portions allow the self-test firmware and hardware to operate for a period of time after which the No. 4 ESS processor resident program checks for accumulated errors. Thus, all self-test routines, checks, and audits are designed to serve as part of the diagnostic, as well as for operational fault detection. In this way, the amount of extra diagnostic code is minimized and failures detected operationally generate useful fault-related data to help repair the unit.

## VII. SUMMARY

We have described a No. 4 ESS hardware subsystem that adds a flexible capability of recording and playing back announcement messages. The subsystem is generally under the control of the No. 4 ESS processor, and has several internal microprocessor systems for control and maintenance purposes. Flexible circuits for interfacing the an-

nouncement system to the No. 4 ESS processor allow for the economical future addition of new equipment. The announcements themselves are stored in digital form on moving-head magnetic disk systems; the organization of the stored data is designed with particular care for easy access during announcement playback. System reliability is a major consideration; error detection, self-test, and diagnostic systems are important components of the subsystem.

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